



Online digital FPGA time-over-threshold trigger system for the HAWC experiment

J. AGUILAR^{1,2}, M. DUVERNOIS¹, T. MONTARULI^{1,2}, I. WISHER², FOR THE HAWC COLLABORATION³

¹University of Wisconsin, IceCube Research Center, Madison, WI 53703

²Department of Physics, University of Wisconsin, Madison, WI 53703

³For full author list see J. Goodman et al., "The HAWC Observatory," these proceedings

duvernois@icecube.wisc.edu

DOI: 10.7529/ICRC2011/V09/1103

Abstract: A very general purpose trigger design for both Xilinx and Altera FPGA architectures was developed for the HAWC gamma ray observatory's PMT signals. This trigger includes several multiplicity triggers implemented over distinct time windows to allow triggering for a wide range of event angles and signal structures in order to allow for the lowest possible gamma ray energy threshold. The trigger includes hardware self-test diagnostics to facilitate matching of selected triggers to PMTs which participated in the trigger. The trigger system allows for a variety of front-end architectures including the HAWC time-over-threshold plus TDC front end system.

Keywords: HAWC, gamma rays, trigger, electronics

1 HAWC Observatory

The HAWC Observatory is a TeV gamma-ray air-shower detector under construction at 4100 m elevation at Sierra Negra, Mexico. It's a high duty-cycle, wide field-of-view telescope sensitive to gamma-rays up to about 100 TeV. The HAWC Detector will consist of a densely packed array of 300 water tank Cherenkov detectors covering an area of about 22,000 m². Each of the 300 tanks is 7.3m in diameter and 4.5 m in height. Three upward looking 20 cm Hamamatsu R5912 PMTs, reused from Milagro, detect the water Cherenkov photons in a dark tank. The PMT signals are run over RG-59cables to Milagro custom-built Front End Boards (FEBs) and the signal edges digitized by Caen V1190 TDCs. In the baseline implementation, these edges are used for triggering in the FPGA-based hardware trigger described in this paper. An alternative design of a software trigger system is also proposed.[1] Further details of the HAWC experiment can be found elsewhere in these proceedings.[2] The construction of the HAWC Observatory will be in phases with the first 30 tanks (90 PMTs) scheduled for data taking beginning in February 2012. This phase, called HAWC30, features the trigger described in this document. The full constructed array (HAWC300) may have a trigger implemented in FPGA hardware or in software.

2 Trigger requirements

The general functional requirements for the trigger are:

1. Form a number of simple multiplicity triggers (SMT) for the 90 PMTs that can return the trigger conditions with well-defined latency. The multiplicity trigger is defined as a digital sum of "hits" within the 25 ns (40MHz) sampling time compared to a threshold. This corresponds to requiring a minimum number of photomultiplier signals above the low discriminator threshold of about 0.2 photoelectrons (*minPMT*) for a certain amount of time ($\Delta t = \text{number of FPGA } 40 \text{ MHz clock cycles above a threshold.}$) The number of SMTs will depend on actual rates and efficiencies of the various triggers.
2. The trigger system will be responsible of providing a trigger mask for each event with flags containing information on which triggers were satisfied in the event.
3. Feedback of the individual channels participating in the trigger for monitoring and for debugging for a prescaled fraction of events.

3 Hardware

For the HAWC30 trigger we have selected a single Terasic Stratix III FPGA[4] evaluation board as the platform for the trigger firmware. Since the FPGA accepts LVDS signals, there will be additional layers of adapter boards for conversion from the ECL signals of the existing FEBs to LVDS. The trigger is mated to the FEBs and Caen VME-based Time to Digital Converters (VX1190 TDCs). Although a VME-based trigger seems like a natural fit into the system,

there are few options with large input counts commercially available. We considered Caen VME-based (V1495) FPGA device but it was too limited for all the requirements above.

3.1 FEBs and TDCs

PMT signals pass through lossy RG-59 high voltage cables and a lightning protection spark gap before entering the data stream in the FEBs. These boards compare the signal levels to thresholds (low threshold at about 0.2 photoelectrons in the tube) and send along digital edges used by the trigger and digitized in the TDC system. The Caen VX1190 TDCs digitize all hits (rising and falling edges) with 100 ps resolution, but these data are read only in the case of a trigger signal being generated from the trigger system.

3.2 Altera Stratix III FPGA Evaluation Board

After trying a number of different FPGA boards, in VME and freestanding, the Terasic [4] DE3 evaluation board was chosen for a good blend of cost effectiveness, high channel count (> 300), FPGA resources, and ease of programmability. Given the limited number of channels (90), ECL to LVDS conversion can be done for HAWC30 with a Caen V1495 FPGA card, and cable/connector adapting done on a custom passive card. For HAWC300, a custom active ECL to LVDS high channel count card system would be built if a hardware trigger is implemented for that phase of the project.

3.3 Connections with other sub-systems

1. Connection to the Front End Board (FEB): the FEB NECL discriminator signals are inputs to a V1495 level adapter (HAWC30) or custom board (HAWC300) that copies them to output for the scaler system and also provides a converted version of the NECL signals in LVDS for input to the trigger system. This conversion is necessary for coupling into the FPGA pin inputs¹. The baseline implementation of the trigger will not use the proportionality of the signal to the amplitude. As a matter of fact, a trigger using it can be potentially more affected by variations of gains in PMTs. Hence, the FPGA will add a fixed duration high state to each TDC edge equal to the time window of the trigger. This will be compared to the performance of a trigger using TOT information as well.
2. Connection to the TDCs: in HAWC30 the trigger signal is sent to a Caen VX1190 VME64X 128 channel multi-hit TDC. TDCs will be operated in the trigger matching mode with readout via MBLT with 10 kByte block sizes. The TDC edges are sent out of the VME crate over a CAEN VME-PCI² that will have a minimum transmission rate between 20

and 40 MB/s. Assuming a (noise) rate per channel of 20 kHz we expect a total maximum rate of $90 \times 20 \times 10^3 \times 4B = 7.2$ MB/s). In the event that the event rate per channel is 40 kHz this number becomes 14.4 MB/s. We estimate that for a threshold of 10 hit channels, in HAWC 30 the trigger rate is about 10 kHz Therefore the TDC output lies below the maximum data rate.

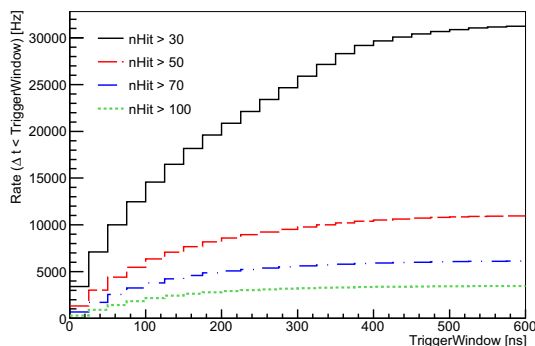


Figure 1: Trigger rates with varying nPMT thresholds and varying trigger windows (Δt).

3. Connection to a 40 MHz system clock and to the GPS absolute clock time: the overall system 40 MHz clock is GPS-derived and is distributed with a custom electronics module to all of the TDCs and to the trigger system. Triggering is synchronous with the 40 MHz clock regardless of internal clock timings within the FPGA which would be derived from the system clock. Absolute clock time (also from GPS) is inserted into one of the TDCs (the one TDC in the HAWC30 phase of the project) and is read with every event trigger via the normal TDC readout.
4. Connection to the calibration system[3]: once the signal is received from the calibration system indicating that the laser is firing the calibration trigger mask is enabled indicating a “light in the detector” condition and initiating a calibration-tagged trigger.
5. Connection to the scaler system: the trigger mask (which triggers are satisfied at a particular time) is sent to the scaler system. Additional multiplicities

1. Each FEB accepts 16 input channels (PMTs) but for symmetry reasons and to minimize the loss of tank hits when a FEB needs to be switched off, the plan is to use 15 of the 16 inputs. Hence, in HAWC 30, 6(= 90 channels /15 channels) front end analog and digital boards receive signals from the 30 tanks and provide an integrated time over threshold output that is used as inputs to the trigger system and to the scaler readout system. The solar output is a variable length NECL signal proportional to the Time-Over-Threshold (TOT) of the signals above the PMT low threshold of about 0.2 photoelectrons (PE) and it extends to include the high threshold TOT when the high threshold is additionally crossed.

2. Caen VX2718 VME64x VME controller to Caen A3818 P-CIE CONET2 readout

(defined as other triggers that are not sent to the TDCs) will also be sent to the scaler system.

6. Connection to the Run Control: pause, stop, busy, debug, and start lines are provided to the trigger system, these lines are controlled by the software in the Run Control system. Start and Stop respectively turn the trigger system on and off. Pause inhibits outgoing triggers, but the trigger system otherwise continues running. Busy does the same but also indicates that the VME readouts, or upstream parts, are in a busy state and not ready for additional data. Debug asserts a debugging condition in which status is reported but experiment triggers are not generated.

Summary of input signals to the trigger:

1. 90 (900 in HAWC300) time-over-threshold (ToT) differential negative emitter coupled logic signals from the FEB;
2. a signal from the calibration system indicating calibration laser light in the detector;
3. 5 Control signals from the Run Control: Stop, Pause, Start, Busy, Debug;
4. 40 MHz system clock signal from GPS;

Provided outputs of the trigger:

- Trigger: This ECL signal is sent to the TDCs, in HAWC 30 there is one line (going to the one TDC) and in HAWC 300 there are eight lines (going to the eight TDC modules). The trigger mask is sent as set of LVDS bits to the scaler system as well as being read out by the trigger DAQ host computer;
- Error: Error conditions are sent out to the trigger DAQ host computer;
- Trigger mask, debug trigger patterns, and trigger timing information are sent to the main data acquisition (DAQ) system.

4 Trigger Algorithms

Two different versions of a SMT trigger were coded the first a simple BigSum with only one step; the other a two step process that takes into consideration the amount of time a threshold is met (TOT). In the second algorithm the first step is a BigSum and the second a TOT. The SOLAR outputs of the FEB are sampled at each 40 MHz-25 ns clock cycle. The BigSum consists of the following steps:

- Sums the signals from the PMTs that went “high” during the clock cycle and therefore generate a number of PMTs hit per clock cycle.

- This number is compared to the number of hit PMTs each clock cycle against multiple preset threshold numbers of PMT hits.

The second step using in the TOT implementation consists in the following steps:

- For each threshold determine whether the condition is met for a required number of clock cycles (“time over threshold”).
- If the timing conditions are met, then output that a trigger has occurred and identify which trigger (threshold and timing) conditions were met.

Aside from these primary calculation steps, the firmware comprises control logic and two different error checking subsystems. Programming is done on an external computer and the firmware is loaded onto the FPGA via industry standard JTAG. Conventional firmware programming practices are followed using manufacturer-specified starting routings, hardware interface layer (HIL), definitions of input and output pins, and automated routing and timing/state analysis of the resulting chip image.

4.1 Error handing & trigger feedback

The control logic is used to coordinate the trigger with the rest of the DAQ. It must accept the signals from the Run Control: Stop, Pause, Debug, Busy, and Start and respond accordingly. The stop command is active low. When it is set the trigger will stop sampling, clear the contents of its onboard memory, and return any triggers still propagating in the system. The start command is active high. When set, it will wait a fixed number of clock cycles and then start nominal trigger operation. The pause signal is active high and temporarily inhibits the trigger generation output. Busy has a similar function, but also passes the information that the DAQ (or upstream computers) are not processing data quickly enough. Debug mode operates the trigger without the full system being present for testing purposes.

The error checking algorithms are setup to check for a number of different problems that might occur. The first algorithm (Redundant SMTs) will check for clock skew errors as well as general failures of the hardware. The second algorithm (Periodic Trigger Sampling) will check to make sure that some select triggers being returned by the trigger system are accurate. Both of these systems will run on-line constantly checking the FPGA for behavioral issues and anomalies. The last algorithm (Offline Pattern Check) will be run off line check the triggers response against a known input checking for errors.

4.2 Trigger testing

Realistic timing patterns, with known proper triggering conditions, are employed in testing the trigger in addition

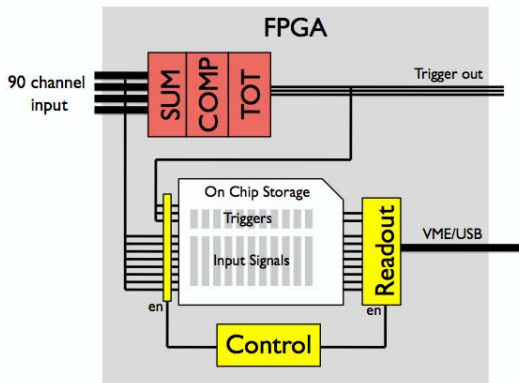


Figure 2: The 2nd trigger implementation with the periodic trigger sampler included.

to the normal timing and state analysis of the chip image logic. The modules that combine to form the trigger are first test individually with unit tests for functionality. Simulated event data (with FEB and cable modeling) can be fed to the trigger chip to understand the detailed trigger performance. Simultaneous running of multiple versions of the trigger can also be used for comparison purposes.

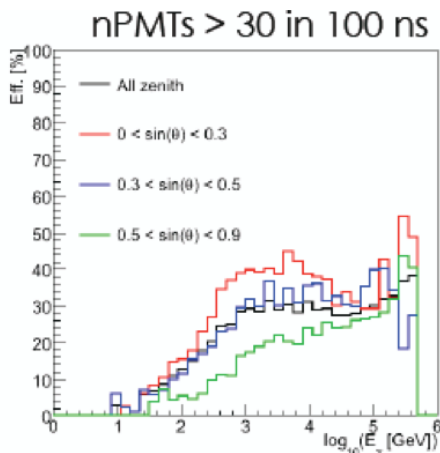


Figure 3: Trigger efficiency for a threshold nPMT = 30 and for trigger window of 100 ns in zenith angle ranges as a function of energy of gammas.

5 Implementation

Since there is a decision on a triggered versus trigger less plan for the full HAWC300, the implementation plan is focused on the HAWC30 stage and a more general purpose path for the hardware trigger. This trigger could then be used for HAWC or other large threshold, or pattern, triggered high-channel count experiments.

The DE3 evaluation board trigger for HAWC30 will be deployed to the counting house at the Mexico site during late 2011 for HAWC30 running beginning in February 2012. The optimized trigger algorithms will be tested on Monte Carlo data prior to deployment, but final versioning is likely to require actual data-taking due to the difficulties in modeling the noise. Any trigger less system could be tried in parallel with the existing trigger as a cross-check. For trigger testing, two hardware copies of the trigger could be employed and compared with the same input signals to check for failures in the hardware.

For an FPGA and ASIC design course at the University of Wisconsin, a 40 nm process ASIC realization of the HAWC trigger was successfully simulated using Design Vision synthesis tools and the *tcbn40lpbwptc* libraries. The design's behavior is verified for clock speeds up to 480 MHz though the actual design has a higher max frequency. The 480 MHz was chosen since this is a speed that would interface easily with the global clock of 40 MHz that is present in HAWC. With more stringent requirements for the synthesis tools, solutions that could run as high as 1.8 GHz were found. This gives a hardware path forward which is not tied to commercial vendors and could be specialized to a HAWC trigger or generalized for broader use.

6 Scalability & future design efforts

The full HAWC300 experiment can be triggered using a trio of the DE3 boards connected together to correlate their subarray subtriggers. This trigger system has a very modest cost. Single FPGA evaluation boards with sufficient inputs for the full experiment were considered to be too expensive and a fully custom solution for an FPGA (or ASIC) trigger were considered to require too much time and development. Although the three board solution is not especially elegant, it does allow for significant modularity of code and construction, and a phased installation. Scaling the system to higher number of PMTs is straightforward due to the modular nature of the DE3. Most of the firmware, written in Verilog, is directly transferable from FPGA platform to platform. A fully custom single board 900+ channel trigger board remains a development possibility based on the firmware designs and modeling of the performance of the design in an ASIC.

References

- [1] J. Pretz *et al.*, (HAWC Coll.), these proc.
- [2] J. Goodman *et al.*, (HAWC Coll.), these proc.
- [3] P. Huentemeyer *et al.* (HAWC Coll.), these proc.
- [4] Terasic, <http://www.terasic.com.tw/>